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384, 410, 408

CLAIMS

What is claimed is:

1. An integrated circuit transistor structure comprising:
   a crystalline semiconductor channel region;
   a gate dielectric overlying said channel region; and
   a conductive gate overlying said gate dielectric, said gate having sidewalls;
   wherein said gate dielectric has thicker portions thereof near said sidewalls of said gate than under central portions of said gate;
   wherein said thicker portions have a thickness contour corresponding to a lateral oxidation from a starting point which is not aligned with said sidewall of said gate, but is interior to said gate.

2. The integrated circuit transistor structure of Claim 1, wherein said gate comprises a metal silicide.

3. A method for forming a transistor gate structure, comprising the steps of:

(a.) forming a dielectric over a semiconductor region;

(b.) forming a patterned gate over said dielectric;

(c.) performing a lateral growth step which increases the thickness of said dielectric in proximity to sidewalls of said gate, but not under central regions of said gate;

(d.) depositing a metallic material onto sidewalls of said gate;

(e.) reacting said metallic material with said gate to form a conductive compound; and

(f.) stripping unreacted portions of said metallic material;

whereby a gate structure with enhanced conductivity is formed.

4. The method of Claim 3, further comprising the step, between said steps (c.) and (d.), of implanting dopants into said semiconductor region near said gate.

5. The method of Claim 3, further comprising the step, between said steps (d.) and (e.), of implanting dopants into said semiconductor region near said gate.

6. A method for forming a transistor gate structure, comprising the steps of:

(a.) forming a dielectric over a semiconductor region;

(b.) forming a patterned gate over said dielectric;

(c.) performing a lateral growth step which increases the thickness of said dielectric in proximity to sidewalls of said gate, but not under central regions of said gate;

(d.) after said step (c.), forming conductive sidewall spacers on said gate.

7. The method of Claim 6, comprising the additional step, after said step (d.), of forming a dielectric spacer on the sidewalls of said gate, to prevent accidental electrical contact to said gate;

8. A product produced by the method of Claim 3.

9. A product produced by the method of Claim 6.